5/A Formal w/ Drwg. 10/31/02

PATENT APPLICATION
Do. No. 5484-093

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Byeong-Hoon LEE, et al.

Serial No. 09/997,080 Examiner: Phan, Trong Q

Filed: November 28, 2001 Group Art Unit: 2818

For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION

Responsive to the Office Action, dated July 22, 2002, please amend the application as follows.

IN THE SPECIFICATION

Please rewrite the paragraph beginning on page 4, line 13, as follows:

A1

A column decoder block 102 is connected to the cell array block 101 to perform a decoding operation. The m number of bit lines are connected to each of the common data lines DLi through a corresponding column decoder. The common data lines include I number of lines DL0 to DLI-1. The common data lines are respectively connected to corresponding write drivers 200, 210 and sense amplifiers 300, 310. All of the source terminals of the memory cell transistors in the cell array block 101 are connected to a common source line SL, driven by the source line driver 500. All of the memory cell transistors are further connected to a common bulk line Bulk at its bulk terminals. The common bulk line Bulk is driven by the bulk driver 400. The transistors T1, T2, T3 in the column decoder block 102 are formed in a separate bulk, which is grounded to 0 V.

Please rewrite the paragraph beginning on page 7, line 7, as follows:

A2

In addition, a plurality of bit lines BL0 to BLm-1 are formed therein, where each of the bit lines BLi is commonly connected to m cell drains. The m bit lines are connected to each of the common data lines DLi through a corresponding column decoder. The common data lines include I lines DL0 to DLI-1. The common data lines are each respectively